Leakage Power Reduction using Multi Threshold Voltage CMOS Technique

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Abstract— In deep sub–micron technology, standby leakage power dissipation has emerged as major design consideration. In this paper, multi threshold voltage CMOS technique for reducing leakage power is proposed. In this technique, the resistance of the path from Vdd to ground is increased, so that significant reduction in static power is achieved with little increase in delay. This work analyses the leakage power and delay of NAND gate and the same can extended to any complex digital implementation. The results are also compared with stacking technique. The circuits are simulated with MOSFET models of level 54 in 90 nm, 45nm and 32nm process technology.

Index Terms— Leakage power, MTCMOS, static power, stacking, sub threshold current, threshold voltage

1 Introduction

As technology scales down to the deep-submicron technology, standby leakage power increases exponentially with the reduction of the supply voltage (V_{dd}) and the threshold voltage (V_{th}). The advances in technology enable us to achieve higher density and performance at the same time results in increase in power consumption. In past day's technology the magnitude of leakage current was low and usually neglected. In current trends, the supply voltage is being scaled down to reduce dynamic power. The threshold voltage also follows the same scaling trend in order to satisfy the high speed requirements.

This decrease of threshold voltages brings an exponential increase in sub-threshold currents [1]. Sub-threshold leakage is the weak inversion current between source and drain of MOS transistor observed when the gate voltage is less than the threshold voltage. Since the leakage current of the transistors determines the static power of a CMOS circuit, the increase in sub-threshold current increases the leakage power consumption of the circuit. Thus the total power consumption of the circuit is increased.

Consequently, power dissipation is becoming recognized as a top priority issue for VLSI circuit design. Leakage power makes up to 50% of the total power consumption in today's high performance microprocessors [2]. Therefore leakage power reduction becomes the key to a low power VLSI design. Leakage power dissipation is the power dissipated by the circuit when it is in sleep mode or standby mode. Leakage power is given by equation 1 and the propagation delay (T_{pd}) of a circuit is given by equation 2.

$$P_{leak} = I_{leak} * V_{dd} \quad (1)$$

$$T_{pd} \propto V_{dd} / (V_{dd}-V_{th})^2 \quad (2)$$

Where I_{leak} is the leakage current that flows in a transistor when it is in off state, V_{dd} is the supply voltage, V_{th} is the threshold voltage of the transistor. This power dominates dynamic power especially in deep submicron circuits and also in circuits that remains in idle mode for a long time such as cell phones. In all such applications, it is important to prolong the battery life as much as possible and now with growing trend towards portable computing and wireless communication, power dissipation has become one of most critical factor in continued development of micro-electronic technology. Therefore the focus is on the reduction of leakage power dissipation.

The rest of the paper is organized as follows, in Section 2, a review of the related work is presented. In Section 3, the proposed work on a leakage reduction for combinational NAND logic gate is presented, which is followed by the simulation results and conclusions in Sections 4 and 5, respectively.

2 Related Work

High leakage current in deep-submicron technology is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. This section reviews different approaches for leakage current reduction techniques. All these techniques are effective in reducing leakage power and ultimately all come down to a fundamental set of concepts: dissipation is reduced by lowering supply voltage, voltage swing, physical capacitance, switching activity or by introduction of a high resistance path between V_{dd} and ground.

In self-adjustable voltage level circuit, the output voltage of the circuit is applied to any load circuit [3]. During the active mode (when SL=0), this circuit supplies maximum supply voltage to the load circuit so that the load circuit can operate quickly. During the standby mode, it provides slightly lower supply voltage to the load circuit through the weakly ON transistors. When drain to source voltage is decreased, the drain induced barrier-lowering (DIBL) effect is decreased and this in turn increases the threshold voltage V_{th} of NMOS transistors. Consequently the sub threshold leakage current of the OFF MOSFETs decreases, so leakage power is minimized, while data are retained.

A technique for leakage power control is Power gating [4], which turns off the devices by cutting off their supply voltage. This technique uses additional transistors (sleep), which are inserted in series between the power supply and pull-up network (PMOS) and/or between pull-down (NMOS) network and ground to reduce the standby leakage currents. The sleep

transistors are turned on when circuit are in active mode and turned off when circuits are in standby mode.

The input vector method makes use of dependence of leakage current on the input vector to gate [5]. Additional control logic is used to put the circuit in a low-leakage standby state when it is idle and restored to its original state when reactivated. Upon reactivation, the circuit no longer retains the original state information before going into low-leakage standby state. Thus, to retain original state information, it requires special latches thereby increasing the area of circuit by about five times in worst cases.

In dual threshold voltage CMOS technique, transistors of different threshold voltages are used. Low threshold voltage transistors are used for the gates on the critical path to maintain the performance, while high threshold voltage transistors are used for the gates on the non-critical path for reduction of the leakage current.

3 Proposed Leakage Reduction Techniques

3.1 MTCMOS Technique

The multi-threshold voltage CMOS (MTCMOS) technique is a kind of power gating technique which uses high threshold transistor as a sleep transistor and low threshold voltage transistors are used to implement the logic [7]. Multi-Threshold CMOS (MTCMOS) is an effective circuit-level methodology that improves the performance in the active mode and saves leakage power during the standby mode. The basic principle of the MTCMOS technique is to use low Vth transistors to design the logic gates where the switching speed is important , while the high Vth transistors also called sleep transistors are used to effectively isolate the logic gates in standby state. The sleep transistors offer the high resistance between supply and ground and limit the leakage dissipation.

Fig. 3.1(a) shows the basic circuit of MTCMOS. The sleep transistor (ST) in MTCMOS circuit is controlled by a sleep control signal. During the standby mode (sleep=1), the ST is off. This causes the leakage current of the logic block to be limited to that of the ST. Due to the high V_{th} of ST, the total leakage of the circuit is minimized. On the other hand, in the active mode (sleep=0), the ST is turned on and the real ground line (GND) is directly connected to the virtual ground line (VGND). Consequently, the low V_{th} logic gates operate normally at a high speed. In the active mode, the sleep transistor works as a resistor as shown in Fig. 3.1(b)

Thus, the introduction of sleep transistor increases the resistance of the path from V_{dd} to ground during standby mode of operation resulting in reduction of leakage current.

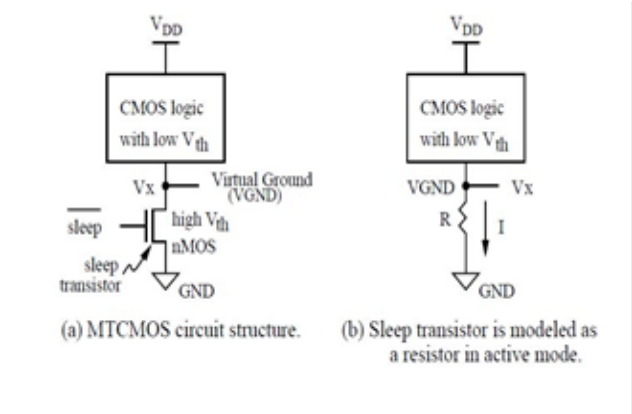

Figure 3.1: Block diagram of MTCMOS circuit structure

3.2 Transistor Stacking

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect".

Sub threshold leakage is exponentially related to the threshold voltage of the device and the threshold voltage changes due to body effect. From these two facts, the sub threshold leakage in the device can reduced by stacking two or more transistors serially. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage [1]. Therefore in Fig. 3.2, transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T1, T2 and T3 is decreased as it flows from V_{dd} to Gnd. So Ileak1 is less than Ileak2.

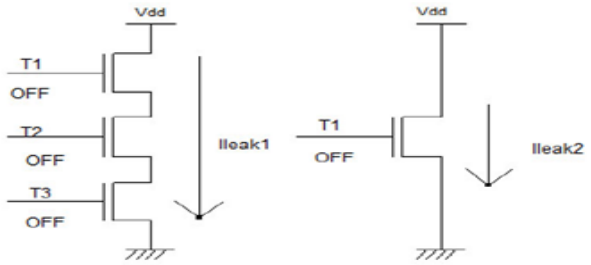

Figure 3.2: Transistor Stacking Effect

4 Simulation and Result

The transistor multi – threshold CMOS and sTACKING techniques were implemented and tested on set of combinational circuits. NAND circuits are implemented and net lists are simulated using Synopsys HSPICE. The implementation of NAND using both the techniques is shown in figure 4.2 and figure 4.3 respectively. Conventional NAND circuit is shown in figure 4.1. All circuits were simulated at a temperature of 25°C. Their leakage power was measured in the standby mode of operation.

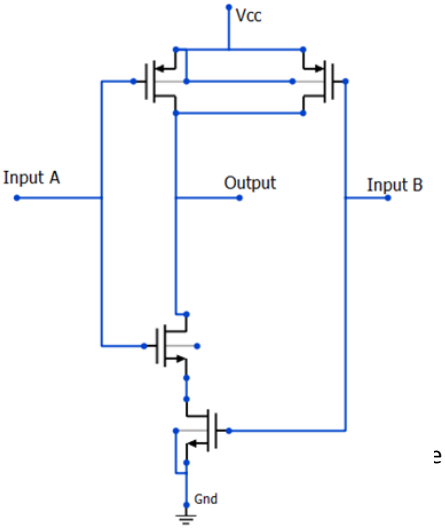

Figure 4.1: Conventional CMOS NAND Gate

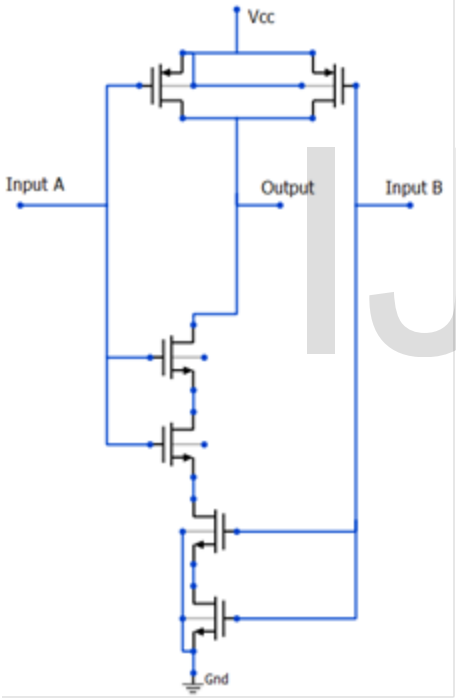

Figure 4.2: Stacked NMOS Transistor NAND

The Berkeley Predictive Technology Models (BPTM) contained process parameters and values for both standard threshold voltage and high threshold voltage devices [10]. The net lists of combinational logic gates are modified with respect to the Berkeley Predictive Technology Models. The modified net lists are also simulated using Synopsys HSPICE for power measurements.

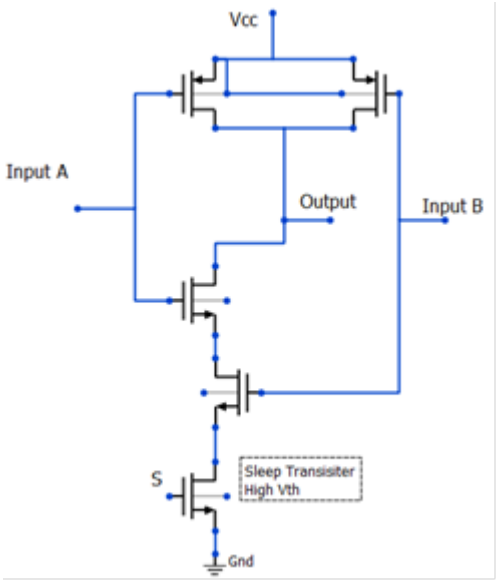

Figure 4.3: MTCMOS NAND Gate

The proposed methods provide exact logic levels and leakage savings as the process technology shrinks. The leakage power measurements are made for the CMOS NAND using 90nm, 45nm and 32nm process technology.

Tables I show the simulation results of NAND circuit for three different process technologies.

From the table I, it is clear that the proposed MTCMOS technique yield more percentage reduction in standby power compared to the stacking technique.

Table I

Standby Leakage power (W) for NAND circuit

Process Technology	Base case	Transistor Stacking	MTCMOS
90n	1.11E-12	0.69E-12	0.531E-12
45n	4.66E-09	1.19E-09	0.073E-09
32n	13.03E-06	5.918E-06	0.066E-06

The proposed techniques achieve significant reduction in standby leakage power with increase in propogation delay. Minimal additional circuitry is used to modify the original logic design to force the combinational logic into a low-leakage state during both active and idle mode of operations. Since the power and delay are inter related, increase in propogation delay is minimum. The same is shown in figure 4.5 for NAND gate.

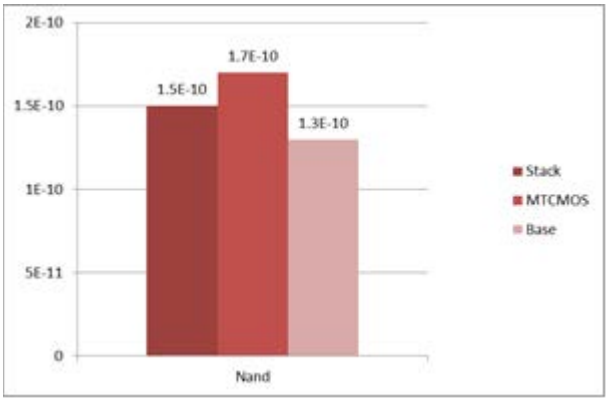

Figure 4.4: Total Leakage Power vs. Process Technology

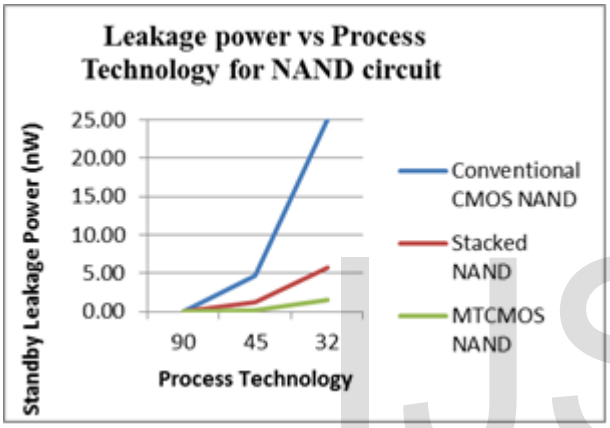

Figure 4.5: Propogation delay for NAND gate

5 Conclusion

Scaling down of the supply voltage and threshold voltage along with CMOS technology feature size for achieving high performance has largely contributed to the increase in standby leakage power dissipation. In this paper, for reducing leakage power efficient technique such as Multi – Threshold voltage CMOS is proposed. The digital circuit NAND gate is implemented with leakage reduction techniques. The leakage power of all the designs decrease when reduction techniques are applied.

The percentage reduction of leakage power is more with the MTCMOS technique compared to the Stacking technique.

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